REMARKS

Upon entry of this amendment, claims 3 and 5-32, as amended, will remain in the application.

Claim Objections

The claims have been amended to obviate the objections.

Claim Rejections – 35 USC § 102

Claims 23, 25, and 27-29 were rejected under 35 U.S.C. 102(b) as being allegedly anticipated by Crouch et al. (U.S. Patent No. 5,617,531, hereinafter "Crouch '531"). Applicant teaches a tiered memory testing architecture including a first tier in which a single, centralized BIST controller is used to control memory tests on multiple memories by issuing generalized commands to sequencers at a second tier, each sequencer associated with memory modules sharing a common clock domain. At the third tier, memory interfaces, each associated with a corresponding memory module, handle specific interface requirements for each memory module, e.g., based on the specific timing requirements and physical characteristics of the memory modules. Advantages of this hierarchical BIST architecture is that area is conserved and overhead for the BIST controller only happens once, whether for testing a couple of memory modules or dozens.

Independent claims 23, 25, and 27 are directed to a centralized BIST controller that controls memory tests on memories having different timing requirements, e.g., organized in subsets in different clock domains or having different access speeds.

In the rejection of claim 23 on page 4, the Action characterizes Crouch '531 as describing a system with a BIST controller and "a plurality of sequencers that are respectively coupled to different subsets of the memory modules (see Crouch '531, column 7 liens 14-24)...and each sequencer controls the application of the test algrorithm to the respective subset of memory modules (see Crouch '531, column 7 lines 56 - column 8 line 18) in accordance with the common clock domain of that subset of memory modules (see Crouch '531, column 9 liens 6-13)." Applicant disagrees with the Action's characterization of Crouch '531 and in particular characterization of the system in the cited passages.

Claim 23 recites, "each sequencer coupled to a different subset of memory modules". However, column 7, lines 14-24 describes the test pattern generator (26) in FIG. 1, which includes a number of sequencers, but there is no indication that different sequencers are associated with different memory subsets.

Claims 23, 25, and 27 recite that at least some of the memories have different timing requirements. The Action cites column 5 lines 7-12 for support that Crouch '531 describes controlling "memory modules with different timing requirements and physical characteristics". However, column 5, lines 7-12 only describes memory modules with different physical characteristics (row depth), but makes no mention of timing requirements. The Action also cites column 9 lines 6-13 for support that Crouch '531 describes controlling application of the test algorithm "in accordance with the common clock domain of that subset of memory modules." However, column 9, lines 6-13 merely states that the bidirectional bus (31) is time multiplexed for sending and receiving data from the memories (12)-(14), but there is no indication that the memories themselves are in different clock domains, and in fact, they are all in the same clock domain.

Crouch '531 does not describe or suggest a system including a centralized BIST controller and a plurality of sequencers for applying test algorithms to memory modules with different timing requirements or residing in different clock domains. Accordingly, Applicant submits that claims 23, 25, and 27, and their dependencies are allowable.

Claim Rejections – 35 USC § 103

Claims 3, 5, 6, 19, 22, 26, and 32 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Crouch '531 in view of Crouch et al. (U.S. Patent No. 5,995,731, hereinafter "Crouch '731").

Claims 7-18, 20, 21, 24, 30 and 31 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Crouch '531 in view of Crouch '731 and in further view of Johnston et al. (U.S. Patent No. 6,272,588, hereinafter "Johnston").

Claims 3, 5-22, 24, 26, 30, and 31 depend respectively from one of allowable independent claims 23, 25, and 27. Accordingly, Applicant submits that these claims are allowable with their base independent claims for the reasons stated above and for their additional limitations.

CONCLUSION

In light of the amendments contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

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